

FIG. 1

(PRIOR ART)

```

module MOD1 (CK1,IN1,IN2,OUT);
  input [width-1:0] CK1;
  input [width-1:0] IN1,IN2;
  output [width-1:0] OUT
  wire [width-1:0] S1,S2,S3,S4,S5
  Reg[width-1:0] R1,R2,R3,R4,R5,R6;
  always @posedge(CK1)
    R1 = S1;
    S1 = R2 & R3;
    R2 = S2;
    S2 = R4 & S5;
    R3 = S3;
    S3 = R1 | R5;
    R4 = S5;
    S4 = IN1 & R6;
    S5 = IN1 | IN2;
    R5 = S4;
    R6 = IN2;
  assign OUT = R1;
endmodule

```

FIG. 2

(PRIOR ART)

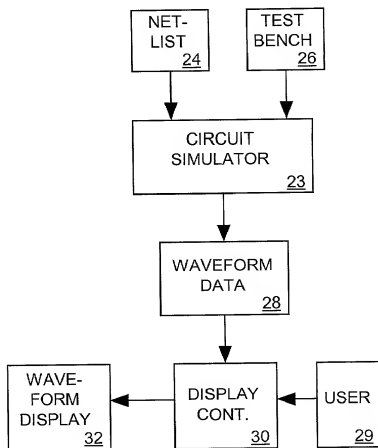


FIG. 3

(PRIOR ART)

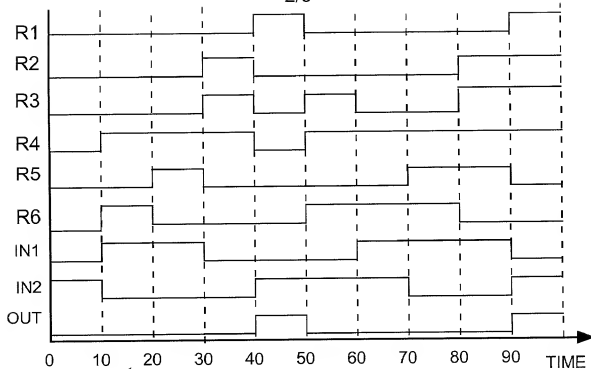


FIG. 4

(PRIOR ART)

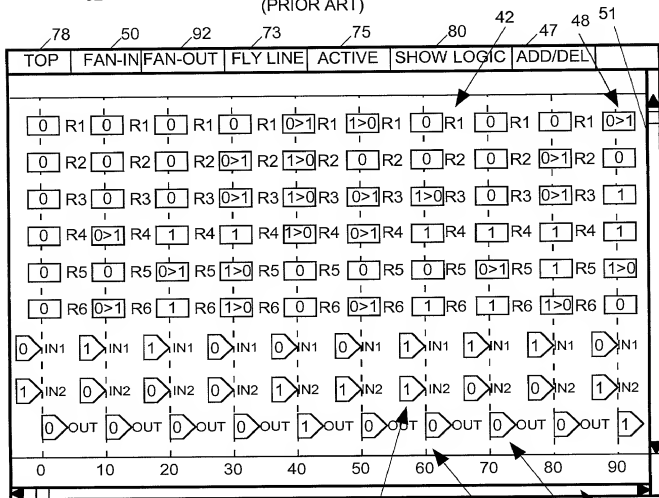


FIG. 5

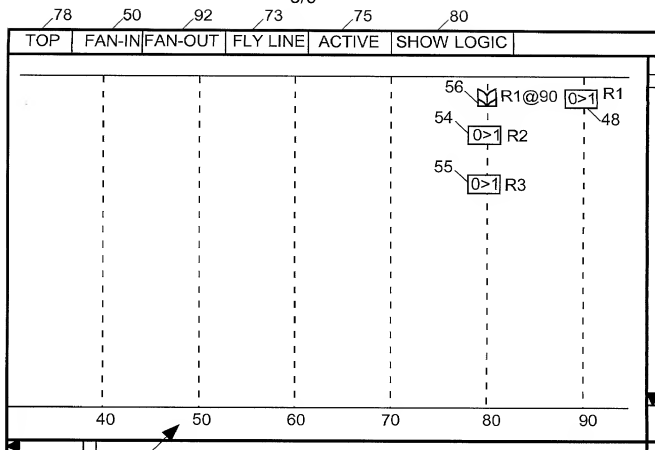


FIG. 6

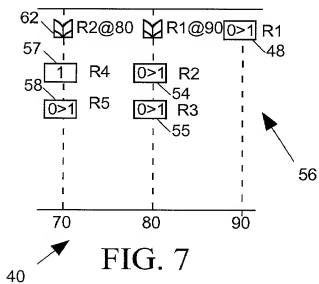


FIG. 7

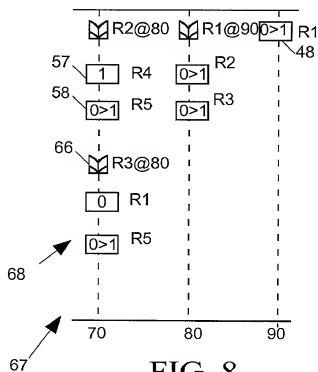
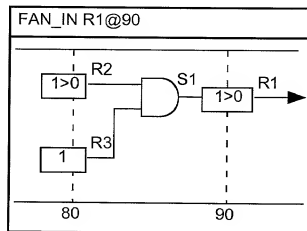
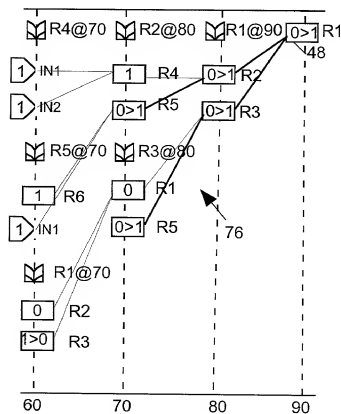
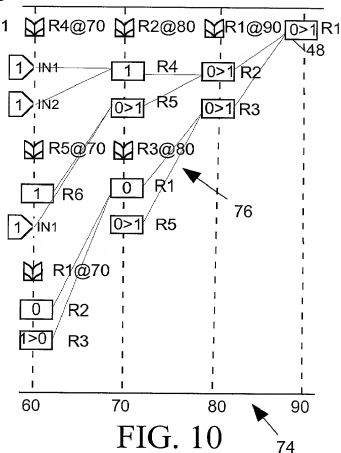
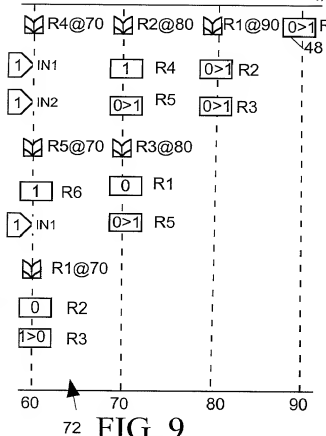


FIG. 8



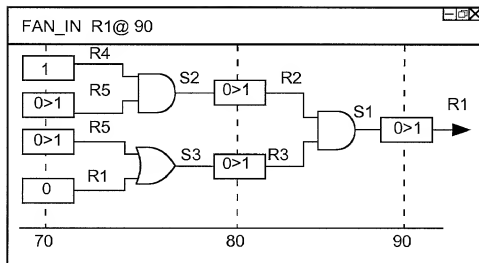


FIG. 13

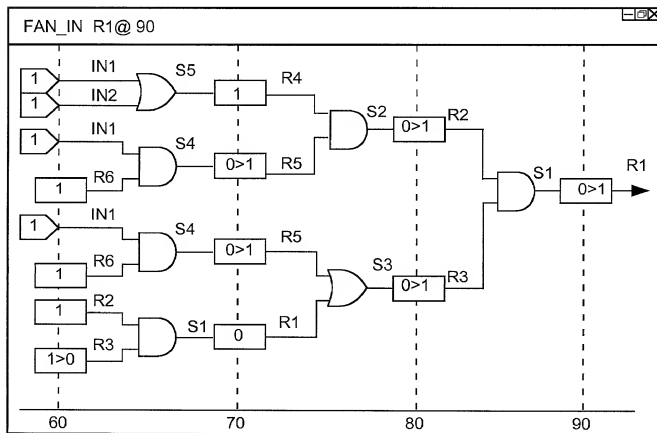


FIG. 14

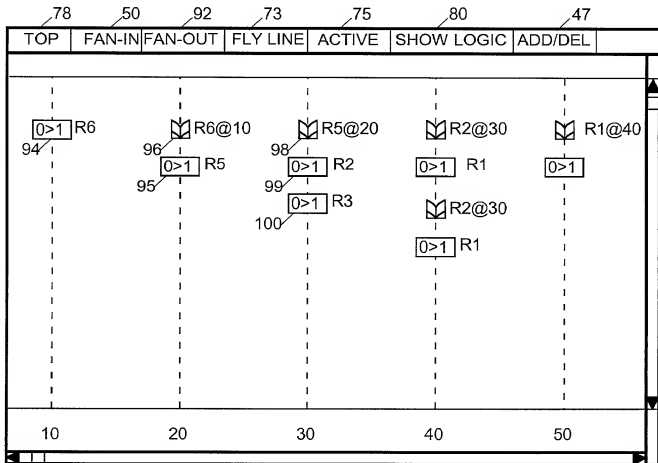


FIG. 15

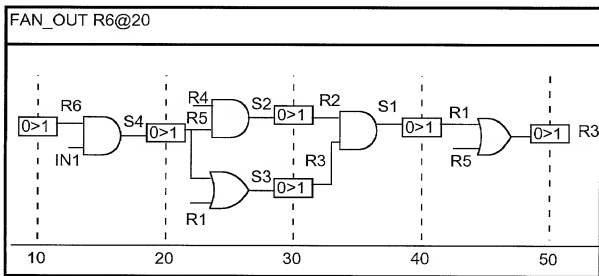


FIG. 16

```

module inet_R2(S2, R4,R5);
  input [width-1:0] R4,R5;
  wire [width-1:0]S2
    S2 = R4 & R5;
endmodule

```

FIG. 19

FIG. 20

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R1: R3
R2: R1
R3: R1
R4: R2
R5: R2, R3
R6: R5

```

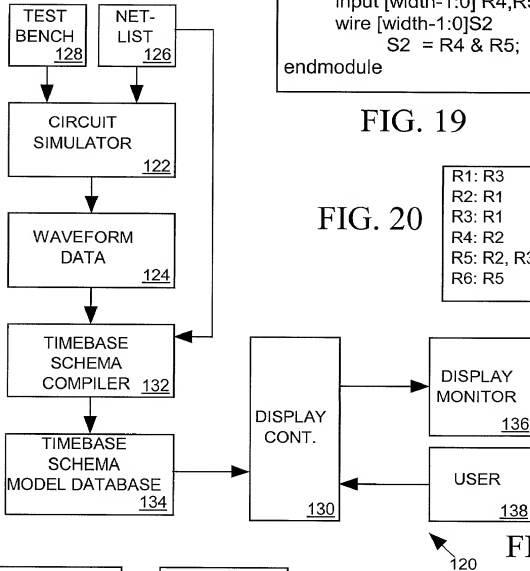


FIG. 17

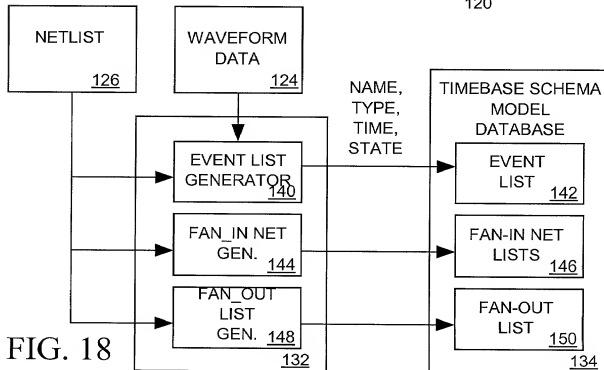


FIG. 18

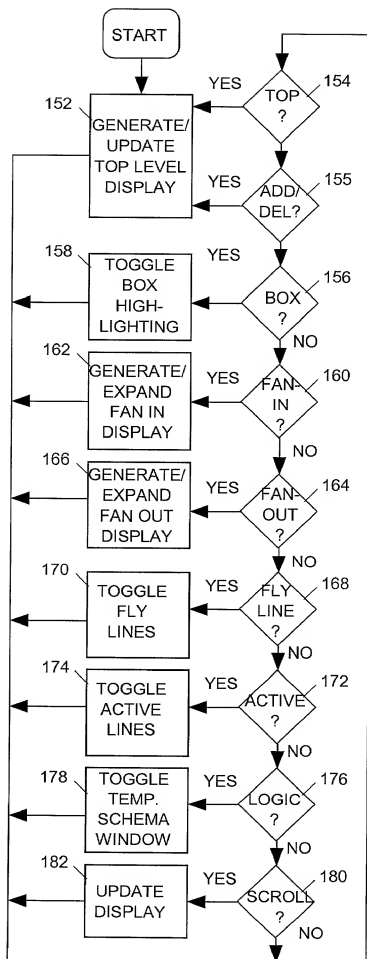


FIG. 21

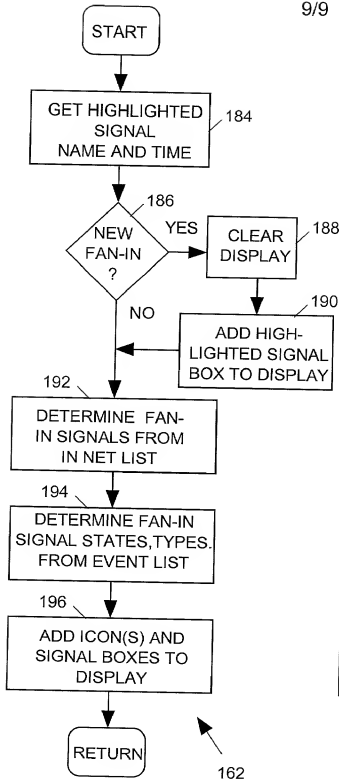


FIG. 22

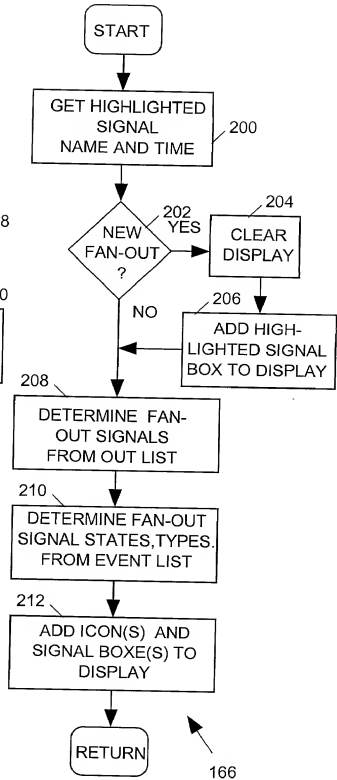


FIG. 23